Please amend the specification as follows:

IN THE SPECIFICATION:

Amend the paragraph beginning at line 24 of page 13 and extending to line 8 of page 14 as follows:

Illustrated in FIG. 10 is a further detail of the memory cell 30 of FIG. 2 wherein the charge storage element layer 40 is implemented by a layer 120 having a single layer of dots, nanoclusters or nanocrystals such as nanocrystal ~~126~~ 122. For the convenience of illustration, elements in FIG. 10 that are equivalent or the same as in FIG. 2 are given the same number. Layer 120 is deposited on the gate dielectric 38 and functions as a charge trapping layer. The gate dielectric 38 is either deposited or grown. Either a single layer or multiple layers of nanocrystals, each with a diameter for example of approximately fifty Angstroms are deposited. All other components of the two bit memory cell, including the control dielectric 42 and the gate electrode 44 are formed as previously described.